

What is claimed is:

1 1. A method of forming a TFT device, comprising the steps
2 of:
3 providing a substrate;
4 performing a first patterning procedure with a first
5 photomask to form a first semiconductor island and
6 a second semiconductor island on part of the substrate;
7 performing a second patterning procedure with a second
8 photomask to expose the first semiconductor island
9 and/or the second semiconductor island;
10 doping impurities into the exposed first semiconductor
11 island and/or the exposed second semiconductor island
12 to adjust threshold voltage;
13 forming an insulating layer on the first semiconductor
14 island, the second semiconductor island and the
15 substrate;
16 forming a conductive layer on the insulating layer;
17 performing a third patterning procedure with a third
18 photomask to remove part of the conductive layer and
19 define a first gate and a second gate;
20 using the first gate and the second gate as a mask, performing
21 an n⁻-ion doping procedure to form an LDD region in
22 the first semiconductor island;
23 performing a fourth patterning procedure with a fourth
24 photomask to expose the second gate;
25 using the second gate as a mask, performing a p⁺-ion doping
26 procedure to form a second source/drain region in the
27 second semiconductor island;

28 forming a passivation layer on the insulating layer, the
29 first gate, and the second gate;
30 performing a fifth patterning procedure with a fifth
31 photomask to form a plurality of contact holes
32 penetrating the passivation layer and the insulating
33 layer; and
34 by means of the contact holes, performing an n^+ -ion doping
35 procedure to form a first source/drain region in the
36 first semiconductor island;
37 wherein an ion dosage of the p^+ -ion doping procedure is
38 greater than an ion dosage of the n^+ ions doping
39 procedure.

1 2. The method according to claim 1, further comprising
2 the step of:
3 filling a conductive material in the contact holes to form
4 a plurality of plugs;
5 wherein the plugs electrically connect the first
6 source/drain region or the second source/drain region.

1 3. The method according to claim 1, further comprising,
2 before forming the first and second semiconductor islands, the
3 step of:
4 forming a buffer layer on the substrate.

1 4. The method according to claim 3, wherein the buffer
2 layer includes a silicon nitride layer and a silicon oxide layer.

1 5. The method according to claim 1, wherein the first and
2 second semiconductor islands include silicon.

1 6. The method according to claim 1, wherein the insulating
2 layer includes a silicon nitride layer and a silicon oxide layer.

1 7. The method according to claim 1, wherein the conductive
2 layer is a metal layer.

1 8. The method according to claim 1, wherein the ion dosage
2 of the p⁺-ion doping procedure is ten times greater than that
3 of the n⁺-ion doping procedure.

1 9. The method according to claim 1, wherein the passivation
2 layer is a silicon nitride layer or a silicon oxide layer.

1 10. A method of forming a CMOS TFT device with five
2 photomasks, comprising steps of:
3 providing a substrate;
4 performing a first patterning procedure with a first
5 photomask to form a first semiconductor island and
6 a second semiconductor island on part of the substrate;
7 performing a second patterning procedure with a second
8 photomask to expose part of the first semiconductor
9 island and/or the second semiconductor island;
10 doping impurities into the exposed first semiconductor
11 island and/or the exposed second semiconductor island
12 to adjust threshold voltage;
13 forming a gate insulating layer on the first semiconductor
14 island, the second semiconductor island and the
15 substrate;
16 forming a conductive layer on the gate insulating layer;
17 performing a third patterning procedure with a third
18 photomask to remove part of the conductive layer and

19 define a first gate and a second gate, wherein the
20 first gate is located above the first semiconductor
21 island and the second gate is located above the second
22 semiconductor island;
23 using the first gate and the second gate as a mask, performing
24 an n⁻-ion doping procedure to form an LDD region in
25 the first semiconductor island;
26 performing a fourth patterning procedure with a fourth
27 photomask to expose the second gate;
28 using the second gate as a mask, performing a p⁺-ion doping
29 procedure to form a second source/drain region in the
30 second semiconductor island;
31 forming a passivation layer on the insulating layer, the
32 first gate, and the second gate;
33 performing a fifth patterning procedure with a fifth
34 photomask, and forming a plurality of contact holes
35 penetrating the passivation layer and the insulating
36 layer, wherein the contact holes are located above
37 the first semiconductor island and the second
38 semiconductor island; and
39 by means of the contact holes, performing an n⁺-ion doping
40 procedure to form a first source/drain region in the
41 first semiconductor island;
42 wherein an ion dosage of the p⁺-ion doping procedure is ten
43 times than that of the n⁺-ion doping procedure.

1 11. The method according to claim 10, further comprising
2 the step of:

3 filling a conductive material in the contact holes to form
4 a first plug, a second plug, a third plug and a fourth
5 plug;

6 wherein the first and second plugs electrically connect the
7 first source/drain region and the third and fourth
8 plugs electrically connect the second source/drain
9 region.

1 12. The method according to claim 10, further comprising,
2 before forming the first and second semiconductor islands, the
3 step of:

4 forming a buffer layer on the substrate.

1 13. The method according to claim 12, wherein the buffer
2 layer includes a silicon nitride layer and a silicon oxide layer.

1 14. The method according to claim 10, wherein the insulating
2 layer includes a silicon nitride layer and a silicon oxide layer.

1 15. The method according to claim 10, wherein the conductive
2 layer is a metal layer.

1 16. The method according to claim 10, wherein the
2 passivation layer is a silicon nitride layer or a silicon oxide
3 layer.